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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,766	11/03/2003	Albert Sun	MXIC 1522-1	4242

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EXAMINER	
PATEL, HETUL B	
ART UNIT	**PAPER NUMBER**
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12/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,766	SUN ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,13-15,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13-15,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to amendment filed on 11/02/2007. Claim 1 is amended; and none of the claims are cancelled or newly added. Therefore, claims 1-10, 13-15 and 18-19 are currently pending in this application.

2. Applicant's arguments filed on 11/02/2007 have been considered but they are not persuasive.

3. The rejection(s) of claims 1-10, 13-15 and 18-19 as in the previous office action is respectfully maintained but updated to show the changes made by the amendment.

Claim Objections

4. Claim 1 is objected to because of the following informalities:

Examiner suggests Applicant to replace the phrase "memory" with either --the memory-- or --said memory-- in line 10 of claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 4-6, 8, 14-15 and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikeda et al. (USPN: 2003/0184339) hereinafter, Ikeda.

As per claim 1, Ikeda teaches an integrated circuit (i.e. the system LSI 10 in Fig. 1) comprising: a configurable logic array (i.e. the Offchip FPGA 14 in Fig. 1) having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array; a programmable non-volatile configuration memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1), adapted to store the configuration data; memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1) storing instructions for a mission function for the integrated circuit, storing instructions for a configuration load function used to receive configuration data via said input port, and storing instructions for a configuration function used to transfer the configuration data to the programmable configuration points within the configurable logic array; the memory (i.e. the ROM 3 in Fig. 1) protected from overwriting or modification by an in circuit programming function i.e. ROM is known to have a built-in function which prevents any modification/overwriting of data stored in it) and storing instructions for a configuration load backup function used to recover from an incomplete transfer of the configuration data from the programmable non-volatile configuration memory to the programmable configuration points within the configurable logic array (i.e. the ROM 3 of the processor 11 in Fig. 1 stores the execution program (object program) (similar to BIOS) which can be re-run incase of the incomplete transfer of data; see paragraph [0052]); and a processor (i.e. the RISC processor 11 in Fig. 1) coupled to the memory which fetches

and executes said instructions from the memory (e.g. see paragraphs [0051]-[0052] and Fig. 1).

As per claims 2 and 4, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1) comprises a nonvolatile read-only memory (i.e. the ROM) (e.g. see Fig. 1).

As per claims 5 and 6, Ikeda teaches the claimed invention as described above. In order to load/receive data from external device(s) and transferring the data within the FPGA, the load function/instruction and the transfer function/instruction has to be stored in the memory so the processor can execute/run it.

As per claim 8, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the configuration function includes loading the programmable non-volatile configuration memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1) via an input port (i.e. shown in Fig. 1 connecting device 2 and 15) on the integrated circuit (e.g. see Fig. 1).

As per claims 14 and 15, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the integrated circuit further comprises an interface (i.e. the combination of 17, 18, 20 and 21 in Fig. 1) between the processor (i.e. 11 in Fig. 1) and the configurable logic array (i.e. 14 in Fig. 1) supporting the configuration function, which loads the programmable non-volatile configuration memory via an input port (i.e. shown in Fig. 1 connecting device 2 and 15) on the integrated circuit (e.g. see Fig. 1); and an interface (i.e. the combination of 17, 18, 20 and 21 in

Fig. 1) between the configuration memory (i.e. 3 in Fig. 1) and the configurable logic array (i.e. 14 in Fig. 1) supporting the transfer of configuration data to the configuration logic array (i.e. 14 in Fig. 1) (e.g. see Fig. 1).

As per claims 18 and 19, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the interface between the programmable non-volatile configuration memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1) and the configuration logic array comprises a dedicated data path (i.e. via 17, 20 and 21 in Fig. 1) including the processor (i.e. 11 in Fig. 1) for said transfer of configuration data to the programmable logic array (i.e. 14 in Fig. 1) (e.g. see Fig. 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Wirtz, II et al. (USPN: 6,414,871) hereinafter, Wirtz.

As per claim 1, Wirtz teaches a system (i.e. the system shown in Fig. 2) comprising: a configurable logic array (i.e. the 24 in Fig. 2) having a programmable configuration defined by configuration data stored in electrically programmable configuration points within the configurable logic array; a programmable non-volatile configuration memory (i.e. 22 in Fig. 1), adapted to store the configuration data; memory

(i.e. the ROM of Host 12 not shown in Fig. 2; it is inherently taught since the host CPU has to have the program memory such as ROM to get the instructions from) storing instructions for a mission function for the integrated circuit, storing instructions for a configuration load function used to receive configuration data via said input port, and storing instructions for a configuration function used to transfer the configuration data to the programmable configuration points within the configurable logic array; and a processor (i.e. the host 12 in Fig. 1) coupled to the memory which fetches and executes said instructions from the memory (e.g. see Col. 8, lines 12+ and Fig. 2).

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Hsu et al. (USPN: 5,359,570) hereinafter, Hsu.

As per claim 3, Ikeda teaches that the memory comprises a nonvolatile read-only memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1). However, Ikeda does not teach that the memory comprises a floating gate memory device. Hsu, on the other hand, teaches that floating gate memory devices have the advantage over using the ROM that they can be programmed and erased, electrically, thereby, exhibiting the advantages of ROM memory, i.e., low power consumption and faster access, along with the writeability of magnetic medium. In addition, as integrated circuit fabrication scale increases, greater density can be achieved. Therefore, it would have been obvious to combine Hsu and Ikeda for the benefits described above.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Sun et al. (USPN: 6,401,221) hereinafter, Sun.

As per claim 7, Ikeda teaches that the claimed invention as described above, but failed to teach the watchdog timer as claimed. Sun, however, discloses a watchdog timer coupled to the CPU (i.e. 122 in Fig. 1), a configuration function that includes using a timer to generate a reset on a response to an error, upon the initialization event, reexecuting the configuration load and configuration function (column 4, lines 15-19). Ikeda and Sun et al. are analogous art because they are from the same field of endeavor, an in circuit programming system that can run downloaded code and reset the system when necessary. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate a watchdog timer and the functions that come with the timer. The suggestion for doing so would have been the ability to reset the system when an error occurs. Therefore, it would have been obvious to combine Sun and Ikeda for the benefit of resetting the system to obtain the invention as specified in claim 7.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Sun et al. (USPN: 5,901,330) hereinafter, Sun2.

As per claim 9, Ikeda teaches that the claimed invention as described above, but failed to teach that the configuration function includes receiving encrypted configuration data via an input port on the integrated circuit, and decrypting the configuration data. Sun2, however, discloses that the configuration function includes receiving encrypted

configuration data via the input port and then decrypting the configuration data (column 13, lines 59-66). Ikeda and Sun2 are analogous art because they are from the same field of endeavor, an in circuit programming system that can run downloaded code and reset the system when necessary. At the time of the invention it would have been obvious to a person of ordinary skill in the art to encrypt the incoming data and then decrypt the data. The suggestion for doing so would have been system security. Therefore, it would have been obvious to combine Sun2 and Ikeda for the benefit of security to obtain the invention as specified in claim 9. The examiner notes that the in-circuit programming and the configuration function perform the same function and are therefore not dissimilar enough to differentiate given the known definitions of the two terms.

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Lawman (USPN: 6,028,445).

As per claim 10, Ikeda teaches that the claimed invention as described above, but failed to teach that the configuration function includes receiving compressed configuration data via an input port on the integrated circuit, and uncompressing the configuration data. Lawman, however, discloses a configuration function that includes receiving compressed configuration data via an input port and then decompressing the data (column 8, lines 12-33). Ikeda and Lawman are analogous ad because both deal with downloading data in a compressed format to a programmable device. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow

the configuration function to receive compressed data and to decompress it. The suggestion for doing so would have been to save time and bandwidth. Therefore, it would have been obvious to combine Lawman and Ikeda for the benefit of time and bandwidth savings to obtain the invention as specified in claim 10.

11. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda.

As per claims 11-13, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the programmable configuration memory comprise floating gate memory cells, i.e. charge programmable memory cells (i.e. the FPGA10 in Fig. 17). However, Ikeda does not clarify whether these cells are volatile or not. However, it is well-known and notorious old in the art at the time the current invention was made to combine both the volatile and nonvolatile cells in the FPGA memory. The common knowledge or well-known in the art statement is taken to be admitted prior art because applicant failed to traverse the examiner's assertion of official notice made in the previous Office Action (see MPEP 2144.03 (C)).

Remarks

12. As to remark, Applicant alleges that none of the cited prior arts teach or suggest that the memory protected from overwriting ormodification by an in circuit programming function and storing instructions for a configuration load backup function as claimed in claim 1.

Examiner respectfully traverses Applicant's remark for the following reasons:

The Ikeda prior art does disclose that the memory (i.e. the ROM 3 in Fig. 1) protected from overwriting or modification by an in circuit programming function i.e. ROM is known to have a built-in function which prevents any modification/overwriting of data stored in it) and storing instructions for a configuration load backup function used to recover from an incomplete transfer of the configuration data from the programmable non-volatile configuration memory to the programmable configuration points within the configurable logic array (i.e. the ROM 3 of the processor 11 in Fig. 1 stores the execution program (object program) (similar to BIOS) which can be re-run incase of the incomplete transfer of data; see paragraph [0052]).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- The patent of US application no: 09/875,599 which is allowed/patented but not published yet, teaches the claimed invention, i.e. a flash memory within an IC which loads data from an external memory to an internal memory and a processor within the IC executes the instruction from the internal memory.

14. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HBP/
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PIERRE BATAILLE
PRIMARY EXAMINER
12/21/07